This is the peer-reviewed version of the article:

Randjelović, B.M., Mitić, V.V., Ribar, S., Lu, C.-A., Radovic, I., Stajcic, A.,

Novakovic, I., Vlahovic, B., 2020. Ceramics, materials, microelectronics and

graph theory new frontiers. Mod. Phys. Lett. B 34, 2150159.

https://doi.org/10.1142/S0217984921501591

Ceramics, materials, microelectronics and graph theory new frontiers

Branislav M. Randjelović[*,†] and Vojislav V. Mitić[*,‡,§]

[*] *Faculty of Electronic Engineering, University of Nis, Nis, Serbia*
[†] *Faculty of Teachers Education, University of K. Mitrovica, Leposavić, Serbia*
[‡] *Institute of Technical Sciences, Serbian Academy of Sciences and Arts, University of Belgrade, Belgrade, Serbia*
[§] *vmitic.d2480@gmail.com*

Srdjan Ribar

Faculty of Mechanical Engineering, University of Belgrade, Belgrade, Serbia

Chun-An Lu

Industrial Technology Research Institute, Hsinchu, Taiwan

Ivana Radovic

Institute of Nuclear Sciences 'Vinča' – National Institute of the Republic of Serbia, University of Belgrade, Belgrade, Serbia

Aleksandar Stajcic

Center of Microelectronic Technologies, Institute of Chemistry, Technology and Metallurgy, National Institute of the Republic of Serbia, University of Belgrade, Belgrade, Serbia

Igor Novakovic

Faculty of Teachers Education, University of K. Mitrovica, Leposavić, Serbia

Branislav Vlahovic

North Carolina Central University (NCCU), Durham, North Carolina, USA

This research is focused on further developing of application and use of graph theory in order to describe relations between grains and to establish control over layers. We used functionalized $BaTiO_3$ nanoparticles coated with Yttrium-based salt. The capacitance change results on super-microstructure levels are the part of the measured values on the

[§]Corresponding author.

bulk samples. The new idea is graph theory application for determination of electronic parameters distribution at the grain boundary and to compare them with the bulk measured values. We present them with vertices in graph, corresponding with grains, connected with edges. Capacitance change with applied voltage was measured on samples sintered in air and nitrogen, up to 100 V. Using graph theory, it has been shown that capacitance change can be successfully calculated on the layers between grains. Within the idea how to get parameters values at microlevel between the grains and pores, mathematical tool can be developed. Besides previously described 1D case, some original calculations for 2D cases were performed in this study, proving successful graph theory use for the calculation of values at nanolevel, leading to a further minituarization in micropackaging.

Keywords: Intergranular capacitance change; graph theory; electronic signal; computing technology.

1. Introduction

Barium titanate ($BaTiO_3$) is considered the most commonly used dielectric in multilayer ceramic capacitors (MLCCs).[1] Therefore, it has been studied extensively from various approaches.[2–8] The ceramic materials synthesis with the grain interface control represents great challenge that could result in material with predetermined functions of synthesized coated grains and thin films. In addition, question of different electrostatic field applications rises, where is important to control parameters on a super level. In order to calculate properties on the grain boundary, we used graph theory,[9–14] based on the values measured on bulk ceramic materials samples.

2. Short Intro into Graph Theory

Graph theory can be easily used for modeling various problems in engineering, technics, mathematics, computer science and in nature.[11] As one of the simplest and most applicable field of mathematics, graph theory has very important advantage among others expressed through the ease of graph algorithms use in solving various problems.[9]

If we map some problems and processes from material science field onto graphs, then it would lead to more efficient simulation of these processes. Graph algorithms and graph operations, as well as parallel algorithms for fast calculations on a large data set, that is typical for multigrain models with a huge number of grains, opening a wide range of new possibilities. Matrices are good and very efficient tool for graph operations and for describing graph properties. Most frequently used graph matrices are adjacency matrix and incidence matrix.[11] Edge connecting graph vertices are used to present intergranular relation; if it's a numerical value, then the edges are assigned number values as well. For beginning, it could be 1 if there is some relation, and 0 if there is no relation.

In a process of multigrain layer integration, which is structured from domains (grains), relation/property between domains is practically integranular capacitance.

Adjacency matrix (usually noted with A) of corresponding graph is usually binary matrix, of dimension $n \times n$, where n is number of vertices (number of grains)

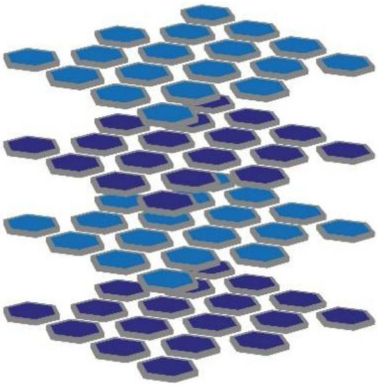


Fig. 1. (Color online) Grains and pores (3D case).

and element of matrix is

$$a_{ij} = \begin{cases} 1, & \text{if there is an edge between vertices } i \text{ and } j\,, \\ 0, & \text{if there is no edges between vertices } i \text{ and } j\,. \end{cases}$$

In this matrix, main diagonal elements are equal to 0 ($a_{ii} = 0$ for $i = 1 \ldots n$).

Incidence matrix (usually noted with B) of corresponding graph is a binary matrix, of dimension $m \times n$, where n is number vertices (grains) and m is number of edges (intergranular capacitance) and element of matrix is

$$b_{ij} = \begin{cases} 1, & \text{if edge } i \text{ is incident with vertex } j \text{ in graph,} \\ 0, & \text{if edge } i \text{ is not incident with vertex } j \text{ in graph.} \end{cases}$$

Incidence matrix is not unique, i.e. it depends on ordering of edges (μ-capacitances). Graph theory can be applied to consolidated grains and pores within the sample structure, like 3D case presented on Fig. 1, or on simpler 2D cases (and 1D cases, as in Ref. 11).

Having in mind that each interconnection or interaction between grains will be mapped onto edge in graph, and that each of them can have some numerical value, it would be useful to use the so-called "weighted" graphs. Weighted graph is graph where each edge has its own numerical characteristic, some "weight". Then instead of adjacency matrix A, we can use "weight" matrix W, of dimensions $n \times n$ too, with elements defined as

$$w_{ij} = \begin{cases} \text{intergranular impedance}, & \text{for } i \neq j \text{ and there is relation between vertices,} \\ 0, & \text{for } i = j \text{ or for } i \neq j \text{ and there is no relation between vertices.} \end{cases}$$

$BaTiO_3$ nanopowder was functionalized with Yttrium salt. The final idea is to calculate dielectric parameter on bilayers between grains, using graph theory and

compare it with the values measured on the bulk ceramic samples. We already introduced this approach in Ref. 5.

In this paper, we will focus on 1D and 2D cases, so we don't need 3D graphs. It is enough that corresponding graphs be planar. Planar graph is graph that is possible to draw on paper, without crossing of edges. Planar graphs have several interesting properties, that could be useful for further analysis. For example, the following equation in Euler's theorem[12]:

$$v - e + f = 2,$$

where v is number of vertices, e is number of edges and f is number of fields (disjunct spaces, lined with edges of graph) in 2D presentation of a graph.

So, planar graphs could be good and flexible mathematical model for analysis and other treatment of layers with grains and pores.

3. Experimental Part

3.1. *Sample preparation*

$BaTiO_3$ — BTO nanoparticles (300 nm) were purchased from SAKAI CHEMICAL INDUSTRY CO., LTD. Modification with Yttrium-organic salt was performed for 1 h at 1300°C and 1350°C in the air and at 1200°C, 1250°C and 1300°C in the reducing atmosphere of N_2. Modified BTO was labeled BTO-Y.

3.2. *Morphological and dielectric characterization*

Morphology of consolidated BTO-Y ceramics was investigated by using field emission scanning electron microscopy (FESEM) (JEOL-JSM-7900F). Sensitivity of the modified BTO on DC bias was measured using KEITHLEY 2400 SourceMeter device.

3.2.1. *FESEM analysis*

Investigation of morphology revealed existence of porous structure in all the samples, which is expected to influence dielectric properties, i.e. DC bias sensitivity. Magnification of 10,000 times showed that samples sintered in air have deeper and larger pores than modified BTO-Y sintered in N_2, but pores are more isolated with clear boundaries.

3.2.2. *Capacitance change with DC bias*

Change of capacitance from 0 V to 100 V of applied voltage has been measured for BTO-Y sintered in air and N_2 atmosphere.

Let us consider experimental results that we obtained, as a starting point for modeling the problem using graph theory. As can be seen in Table 1, with the rise of sintering temperature, capacitance value begins to increase instead of decreasing.

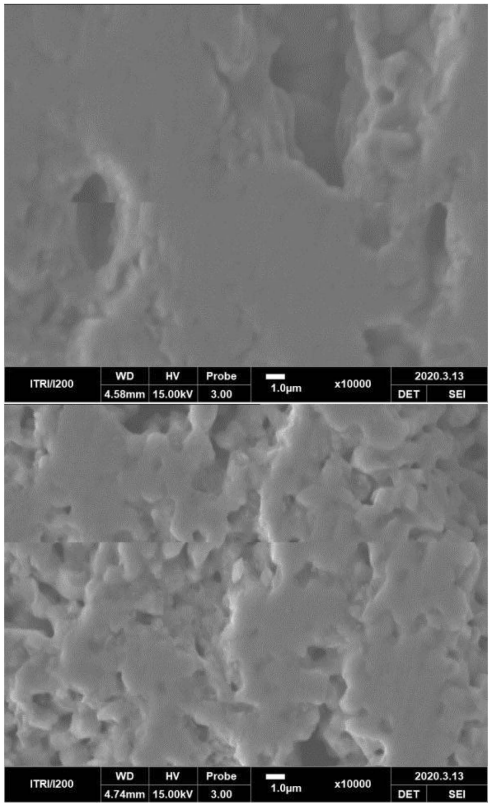


Fig. 2. Sample BTO-Y sintered in: air (left) and N_2 (right).

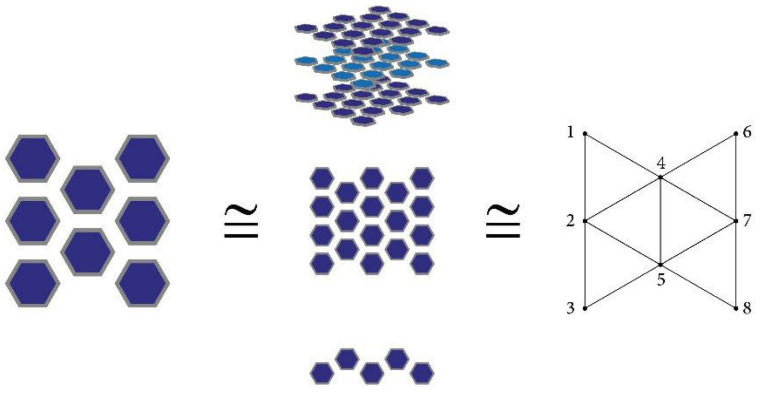
Table 1. Expermiental results of capacitance change with DC bias BTO-Y sintered in N_2 at temperatures 1200°C, 1250°C and 1300°C.

DC Bias, V	Temp.	0	10	20	30	40	50	60	70	80	90	100	
	1200	0.036	0.721	2.01	0.736	0.457	−0.102	−0.878	−1.842	−2.852	−3.985	−5.073	Capacitance
	1250	0.022	1.762	5.52	3.252	3.646	3.887	4.065	4.207	4.297	4.369	4.377	change,
	1300	0.038	1.318	4.265	2.696	2.804	2.976	3.048	3.102	3.138	3.156	3.156	%

For the BTO-Y sintered in air, only one value was taken for the purpose of graph theory application, voltage of 40 V that induced capacitance decrease of 5.065%.

3.3. *Theoretical experiment*

Starting from the results of measures, performed on a bulk sample, we will use 3D structure of synthesized ceramic material and present it as 1D and 2D case, with help of graph theory in parameters at grain boundary calculation. This idea is presented on Scheme 1.



Scheme 1. (Color online) Presentation of structure and application of graph theory.

In this research, we will use 2D case, instead 3D, without loss of generality. This 2D case could be, later, easily generalized and mapped onto some 3D case. We will investigate and discuss application of graph theory on sintered samples and also their electrical characterization.

The first step is to introduce graph theory as a mapping tool to define parameters of the analyzed process. Let's discuss sintered consolidated structure and appropriate graph structure, where any relation between neighboring cells could be expressed by value that will be weight of the edge of this graph.

If we take into consideration obtained experimental results for capacity change given in Sec. 2.2.2, and then create graph model for 2D case, we will apply graph theory to sintered elements like this 3D case (Fig. 3). or its simplification to 2D case (Fig. 4):

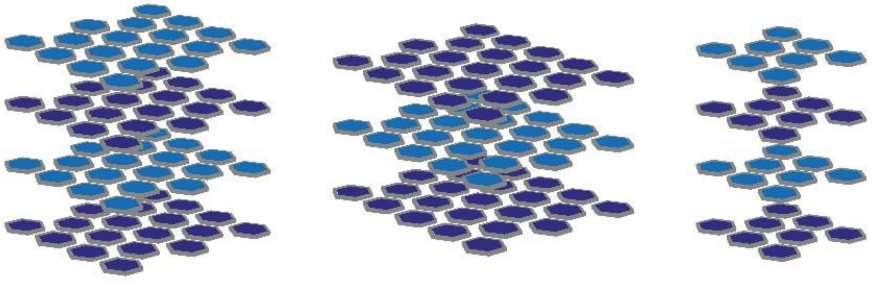


Fig. 3. (Color online) Structure of grains (according to 3D case).

Fig. 4. (Color online) Structure of grains (according to 2D case).

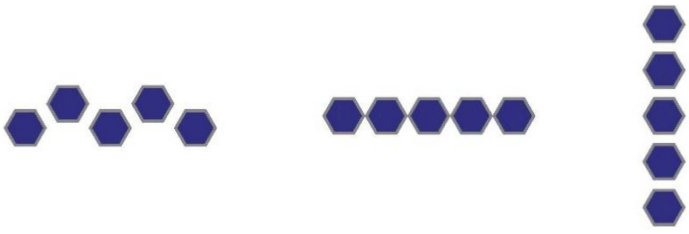


Fig. 5. (Color online) Structure of grains (according to 1D case).

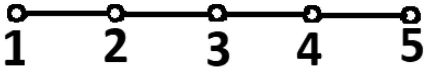


Fig. 6. Graph for 1D case.

In order to establish appropriate theoretical experiment, through which we will model this sintered sample, where plate is represented with graph, we will simplify cases, and instead of 2D case, we will begin with one of 1D case, as in Ref. 11. This is shown in Fig. 5.

We will construct graph from some of those cases, for example the last one (vertical arrangement and horizontal arrangement) with $n = 5$ and $n = 8$ grains. Our aim is that the model has same overall results in relative change of capacitance, in relation with those (measured) overall results.

4. Results and Discussion

Successful coating of $BaTiO_3$ nanoparticles could improve its dielectric properties, and it represents an important step towards downsize parameter control. Next to the synthesis, successful calculations and prediction of electronic parameters at grain level proved to be necessary for the complete parameter control. When graph theory is applied, grains are presented as vertices and capacitance values at grain boundary as edges. In this manner, graph theory can be used for characterization of ceramic capacitors, in this study, BTO-Y with the potential use in MLCC. Formation of a new phase between grains influences dielectric behavior of the bulk material, which can be investigated through the relative capacitance change with applied voltage, i.e. DC bias sensitivity. Graph structures, mimicking ceramics, were presented as 1D and 2D cases (Figs. 4 and 5), with Eqs. (1) and (2). Five grain matrix with adequate correspondent equations (1)–(3) was used.

Graphs with the same number of vertices ($n = 5$), so we will divide overall capacitance change to a local measure, between two grains. For example, for $n = 5$ and for DC bias of 40 V, applied on BTO sintered at $t = 1300°$ in N_2, we have overall capacity change of 2.804. This means that between neighboring vertices in

graph, we have capacity change $\frac{\Delta C}{C}$ of

$$\frac{\Delta C}{C} = \frac{2.804}{n-1} = \frac{2.804}{4} = 0.701. \tag{1}$$

Appropriate weight matrix of this graph (for $n = 5$) is

$$W = \begin{bmatrix} 0 & 0.701 & 0 & 0 & 0 \\ 0.701 & 0 & 0.701 & 0 & 0 \\ 0 & 0.701 & 0 & 0.701 & 0 \\ 0 & 0 & 0.701 & 0 & 0.701 \\ 0 & 0 & 0 & 0.701 & 0 \end{bmatrix}.$$

In that case, we have parallel connection of capacity changes, and overall capacity change is equal to 2.804.

If we use different planar graph, that is isomorphic with previous one, also with $n = 5$, but with "vertical" arangment of graph nodes, then we can calculate "weight" of each node as serial connection of capacities, so capacity change $\frac{\Delta C}{C}$ between neighboring vertices in graph

$$\frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} = \frac{1}{2.804} => \frac{\Delta C}{C} = 5 \cdot 2.804 = 14.020. \tag{2}$$

Appropriate weight matrix of this graph (for $n = 5$) is

$$W = \begin{bmatrix} 0 & 14.020 & 0 & 0 & 0 \\ 14.020 & 0 & 14.020 & 0 & 0 \\ 0 & 14.020 & 0 & 14.020 & 0 \\ 0 & 0 & 14.020 & 0 & 14.020 \\ 0 & 0 & 0 & 14.020 & 0 \end{bmatrix}.$$

In that case, we have serial connection of capacity changes, and overall capacity change is again equal to 2.804.

For $n = 5$ and for 40 V applied on BTO modified in air on 1350°C, which was taken for comparison, we have the overall capacity change of -5.065. This means that between neighboring vertices in graph we have capacity change $\frac{\Delta C}{C}$ of

$$\frac{\Delta C}{C} = \frac{-5.065}{n-1} = \frac{-5.065}{4} = -1.26625. \tag{3}$$

Appropriate weight matrix of this graph (for $n = 5$) is

$$W = \begin{bmatrix} 0 & -1.26625 & 0 & 0 & 0 \\ -1.26625 & 0 & -1.26625 & 0 & 0 \\ 0 & -1.26625 & 0 & -1.26625 & 0 \\ 0 & 0 & -1.26625 & 0 & -1.26625 \\ 0 & 0 & 0 & -1.26625 & 0 \end{bmatrix}.$$

In that case, we have parallel connection of capacity changes, and overall capacity change is equal to -5.065.

If we use different planar graph, that is isomorphic with previous one, also with $n = 5$, but with "vertical" arangment of graph nodes, then we can calculate "weight" of each node as serial connection of capacities, so capacity change $\frac{\Delta C}{C}$ between neighboring vertices in graph

$$\frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} = \frac{1}{-5.065} => \frac{\Delta C}{C} = -5 \cdot 5.065 = -25.325. \quad (4)$$

Appropriate weight matrix of this graph (for $n = 5$) is

$$W = \begin{bmatrix} 0 & -25.325 & 0 & 0 & 0 \\ -25.325 & 0 & -25.325 & 0 & 0 \\ 0 & -25.335 & 0 & -25.325 & 0 \\ 0 & 0 & -25.325 & 0 & -25.325 \\ 0 & 0 & 0 & -25.425 & 0 \end{bmatrix}.$$

In that case, we have serial connection of capacity changes, and overall capacity change is again equal to -5.065.

Let us make graph from one of 2D cases, for example with $n = 8$ graines. So, we have graph with same number of vertices ($n = 8$) and $m = 13$ edges. Suppose that we can divide overall capacitance change to local measure that characterizes relation between two grains (two vertices in graph). For example, for $n = 5$ and for DC bias of 80 V, with sample sintered on temperature$t = 1250°$, we have overall capacity change of 4.297. This means that for $n = 8, m = 13$ and for between neighboring vertices in graph we have capacity change $\frac{\Delta C}{C}$ of

$$\frac{\Delta C}{C} = \frac{4.297}{n-1} = \frac{4.297}{12} = 0.3583. \quad (5)$$

Appropriate weight matrix of this graph is

$$W = \begin{bmatrix} 0 & 0.3583 & 0 & 0.3583 & 0 & 0 & 0 & 0 \\ 0.3583 & 0 & 0.3583 & 0.3583 & 0.3583 & 0 & 0 & 0 \\ 0 & 0.3583 & 0 & 0 & 0.3583 & 0 & 0 & 0 \\ 0.3583 & 0.3583 & 0 & 0 & 0.3583 & 0.3583 & 0.3583 & 0 \\ 0 & 0.3583 & 0.3583 & 0.3583 & 0 & 0 & 0.3583 & 0.3583 \\ 0 & 0 & 0 & 0.3583 & 0 & 0 & 0.3583 & 0 \\ 0 & 0 & 0 & 0.3583 & 0.3583 & 0.3583 & 0 & 0.3583 \\ 0 & 0 & 0 & 0 & 0.3583 & 0 & 0.3583 & 0 \end{bmatrix}.$$

This results to overall capacitance change equal to 4.297.

If we use different planar graph, that is isomorphic with previous one, also with $n = 8$, but with "vertical" arangment of graph nodes, then we can calculate

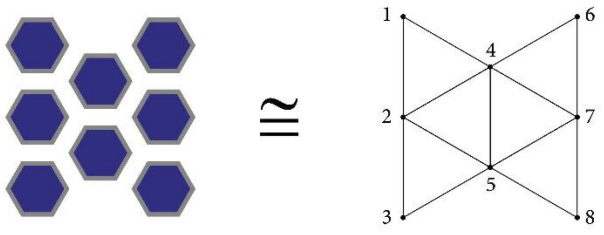


Fig. 7. (Color online) 2D case.

"weight" of each node as serial connection of capacities, so capacity change $\frac{\Delta C}{C}$ between neighboring vertices in graph

$$\frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} + \cdots + \frac{1}{\frac{\Delta C}{C}} + \frac{1}{\frac{\Delta C}{C}} = \frac{1}{4.297} => \frac{\Delta C}{C} = 8 \cdot 4.297 = 34.376. \tag{6}$$

Appropriate weight matrix of this graph (for $n = 8$) is

$$W = \begin{bmatrix} 0 & 34.376 & 0 & 34.376 & 0 & 0 & 0 & 0 \\ 34.376 & 0 & 34.376 & 34.376 & 34.376 & 0 & 0 & 0 \\ 0 & 34.376 & 0 & 0 & 34.376 & 0 & 0 & 0 \\ 34.376 & 34.376 & 0 & 0 & 34.376 & 34.376 & 34.376 & 0 \\ 0 & 34.376 & 34.376 & 34.376 & 0 & 0 & 34.376 & 34.376 \\ 0 & 0 & 0 & 34.376 & 0 & 0 & 34.376 & 0 \\ 0 & 0 & 0 & 34.376 & 34.376 & 34.376 & 0 & 34.376 \\ 0 & 0 & 0 & 0 & 34.376 & 0 & 34.376 & 0 \end{bmatrix}.$$

In that case, we have serial connection of capacity changes, and overall capacity change is again equal to 4.297.

5. Outlook

In the future research, complex 3D cases will be developed, enabling the full insight in parameters change, from bulk to grain level. Due to a great influence of porosity on electronic properties, especially on total and integral capacitance, we will continue to develop graph theory application between pores. Furthermore, graph theory will be applied combined with neural networks calculations, in order to compare obtained results from different approaches and get wider image of the material's properties.

6. Conclusion

Graph theory was applied for calculation of intergranular dielectric properties $BaTiO_3$ ceramics modified with Yttrium based salt. DC bias sensitivity can be

influenced by the change in sintering temperature, leading to an increase in capacitance value with the applied voltage. Relative capacitance change measured on the bulk samples, depending on the sintering temperature was downsized to a granular level using graph theory approach. 1D and 2D cases are developed, showing that the bulk parameters were successfully calculated on a granular interface. In this manner, classical microstructural and dielectric analyses were enriched with a new insight in the properties of the synthesized sample. Complete parameter control can be achieved if calculations from graph theory are combined with different characterization methods These further steps will be in focus of our next research and scientific papers reports. Introduction of such powerful mathematical tool in the materials science gives researchers the opportunity for more thorough investigation of synthesized materials, and potential for prediction of dielectric properties that leads to a more efficient production and miniaturization of electronic devices.

References

1. Y. Slimani, B. Unal, E. Hannachi, A. Selmi, M. A. Almessiere, M. Nawaz, A. Baykal, I. Ercan and M. Yildiz, *Ceram. Int.* **45** (2019) 11989.
2. S. F. Wang, Y. F. Hsu, Y. W. Hung and Y. X. Liu, *Appl. Sci.* **5** (2015) 1221.
3. Z. Shen, X. Wang, H. Gong, L. Wu and L. Li, *Ceram. Int.* **40** (2014) 13833.
4. A. Guzu, C. E. Ciomaga, M. Airimioaei, L. Padurariu, L. P. Curecheriu, I. Dumitru, F. Gheorghiu, G. Stoian, M. Grigoras, N. Lupu *et al.*, *J. Alloys Compd.* **796** (2019) 55.
5. Y. Sato, M. Aoki, R. Teranishi, K. Kaneko, M. Takesada, H. Moriwake, H. Takashima and Y. Hakuta, *ACS Appl. Nano Mater.* **2** (2019) 5761.
6. Ł. Zych, A. Wajler and A. Kwapiszewska, *J. Ceram. Sci. Technol.* **7**(3) (2016) 277.
7. W.-G. Yang, B.-P. Zhang, N. Ma and L. Zhao, *J. Eur. Ceram. Soc.* **32** (2012) 899.
8. Z. Liu, Z. Xing, H. Wang, Z. Xue, S. Chen, G. Jin and X. Cui, *J. Alloys Compd.* (2017), doi:10.1016/j.jallcom.2017.08.175.
9. R. V. Rao, *Mater. Sci. Eng.* **431**(1–2) (2006) 248.
10. J. A. Anderson, *Discrete Mathematics with Combinatorics* (CET, Cacak, Serbia, 2005) (in Serbian).
11. B. M. Randjelović and Z. S. Nikolić, A mathematical model for simulation of intergranular μ-capacitance as a function of neck growth in ceramic sintering, in *Computational Mathematics and Variational Analysis*, Springer Optimization and Its Applications, Vol. 159, eds. N. Daras and T. Rassias (Springer, Cham, 2020), pp. 403–420.
12. B. M. Randjelović and Z. S. Nikolić, Graph theory applied to modeling and simulation of microstructure evolution in sintering (Invited Lecture INV-MS 3), in *Advanced Ceramics and Applications VIII: New Frontiers in Multifunctional Material Science and Processing*, Book of Abstracts, eds. V. Mitić, L. Mančić and N. Obradović (Serbian Ceramic Society, Belgrade, 2019), p. 38, ISBN: 978-86-915627-7-9.
13. V. V. Mitić, G. Lazović, B. M. Randjelović, V. Paunovic, I. Radovic, A. Stajcic and B. Vlahovic, *Ferroelectrics* **570**(1) (2021).
14. V. V. Mitić, G. Lazović, B. M. Randjelović, V. Paunović, J. M. Wu, D. Mancić and J. R. Hwu, Fractal microeletronic frontiers and graph theory applications, *Int. Conf. MS & T 2019*, Book of Abstracts, Portland, USA, 29 September–3 October 2019.